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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,697	06/28/2001	Kiyoshi Hidaka	210287US2	4677

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EXAMINER	
ANYASO, UCHENDU O	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,697	HIDAKA ET AL.	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3, 4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1-20** are pending in this action.

Claim Rejections - 35 USC ' 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 10-12** and **20** are rejected under 35 U.S.C. 102(b) as being anticipated by *Selwan* (U.S. Patent 5,526,025).

Regarding **independent claims 10** and **20,** Selwan teaches a semiconductor device for driving liquid crystals (column 11, lines 36-38) comprising: a single-port memory that stores display-data as represented by display memory read FIFO to be displayed on a liquid crystal displaying section (column 18, lines 40-44).

Furthermore, Selwan teaches a first latch circuit 1212 that stores the display-data from the single-port memory 1210 in response to a first latch signal; and a second latch circuit 1214 that stores an output of the first latch circuit in response to a second latch signal, and wherein the controller 1210 outputs the first latch signal based on the second latch signal and a CPU-access signal that indicates the access operation of the CPU to the single-port memory (see figure 12 at 1210, 1212, 1214).

Also, Selwan teaches a controller 1220 that generates a latch control signal and sends the latch control signal to the latch circuit, the latch control signal being generated based on a CPU-

access signal (see block 1222) indicating an access operation of a CPU to the single-port memory and a specific signal that is synchronized with a display-data retrieval cycle for the liquid crystal driver (see column 17, lines 50-57).

Regarding **claims 11** and **12**, in further discussion of claim 10, Selwan teaches a first latch circuit 1212 that stores the display-data from the single-port memory 1210 in response to a first latch signal; and a second latch circuit 1214 that stores an output of the first latch circuit in response to a second latch signal, and wherein the controller 1210 outputs the first latch signal based on the second latch signal and a CPU-access signal that indicates the access operation of the CPU to the single-port memory (see figure 12 at 1210, 1212, 1214).

Claim Rejections - 35 USC ' 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-9** and **13-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Selwan* (U.S. Patent 5,526,025) in view of Shimomura (U.S. 6,333,745).

Regarding **independent claims 1** and **19,** and for **claim 2,** Selwan teaches a semiconductor device for driving liquid crystals (column 11, lines 36-38) comprising: a single-port memory that stores display-data as represented by display memory read FIFO to be displayed on a liquid crystal displaying section (column 18, lines 40-44).

Furthermore, Selwan teaches how a liquid crystal driver retrieves the display-data stored in the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section by teaching that when display memory read FIFO 1212 starts filling up, data is input into holding latch 1214 such that when holding latch 1214 has valid data in it, FIFO control circuit block 1220 clocks data into pixel FIFO 1244 and into Down Counter 1216 (see figure 19, lines 58 through column 20, line 2, figure 12).

Also, Selwan teaches how load signal 1246 indicates whether data is being loaded into pixel FIFO 1244 such that when data is being loaded into pixel FIFO 1244, down counter 1216 decrements its value by 1 wherein each time new data is latched into Pixel FIFO 1244, the down counter 1216 is decremented and when down counter 1216 reaches a value of (-1), a new data value is latched into holding latch 1214 and a new tag value is latched into down counter 1216 (column 19, lines 56 through column 20, line 2).

Also, Selwan teaches how the display data is piped from the holding latch 1214 to the Pixel FIFO 1244 and based on the load signal from the FIFO control 1220 this display data is piped to the LCD/CRT via the Attribute Controller and the CRT interface (*see* figure 12).

However, Selwan does not teach how priority is given to CPU when the CPU has access to memory while data is being retrieved from the memory to the liquid crystal driver. On the other hand, Shimomura teaches a data processing system comprising: a CPU; a memory for storing programs and display data; a memory controller connected to said CPU via a CPU bus and said memory via a memory bus, **for providing priority** to an access request from said CPU to said memory, said memory controller having a display controller for reading the display data stored in said memory, and a buffer for storing an access request from said display controller to

said memory, and execution of the memory access by said display controller in response to an access request from said CPU (column 34, lines 55-67).

Thus, it would have been obvious to combine Selwan and Shimomura because while Selwan teaches how a liquid crystal driver retrieves the display-data stored in the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section by teaching that when display memory read FIFO 1212 starts filling up, data is input into holding latch 1214 such that when holding latch 1214 has valid data in it, FIFO control circuit block 1220 clocks data into pixel FIFO 1244 and into Down Counter 1216 (see figure 19, lines 58 through column 20, line 2, figure 12), Shimomura teaches how priority is given to CPU when the CPU has access to memory by means of a memory controller connected to said CPU via a CPU bus and said memory via a memory bus, **for providing priority** to an access request from said CPU to said memory, said memory controller having a display controller for reading the display data stored in said memory, and a buffer for storing an access request from said display controller to said memory, and execution of the memory access by said display controller in response to an access request from said CPU (column 34, lines 55-67). The motivation for combining these inventions would have been to prevent performance degradation due to waiting of the CPU for access to the main memory (column 3, lines 11-16).

Regarding **claims 3** and **4**, in further discussion of claim 1, Selwan teaches a first latch circuit 1212 that stores the display-data from the single-port memory 1210 in response to a first latch signal; and a second latch circuit 1214 that stores an output of the first latch circuit in response to a second latch signal, and wherein the controller 1210 outputs the first latch signal

based on the second latch signal and a CPU-access signal that indicates the access operation of the CPU to the single-port memory (see figure 12 at 1210, 1212, 1214).

Regarding **claims 5-7**, in further discussion of claim 3, Shimomura teaches a data processing system comprising: a CPU; a memory for storing programs and display data; a memory controller connected to said CPU via a CPU bus and said memory via a memory bus, **for providing priority** to an access request from said CPU to said memory, said memory controller having a display controller for reading the display data stored in said memory, and a buffer for storing an access request from said display controller to said memory, and execution of the memory access by said display controller in response to an access request from said CPU (column 34, lines 55-67).

Furthermore, Shimomura teaches in FIG. 9, how the transfer time register 910, the transfer time (delay time) of the first command from the CPU bus 131 to the memory bus 135 which is generated by the memory interface circuit 152 of the memory controller 140 when access from the CPU 100 is generated while the memory bus 135 is used by the display controller 156 or the rendering processor 157 is registered (column 13, lines 45-53, figure 9).

Regarding **claim 8**, in further discussion of claim 3, Shimomura teaches in FIG. 9, how the transfer time register 910, the transfer time (delay time) of the first command from the CPU bus 131 to the memory bus 135 which is generated by the memory interface circuit 152 of the memory controller 140 when access from the CPU 100 is generated while the memory bus 135

is used by the display controller 156 or the rendering processor 157 is registered (column 13, lines 45-53, figure 9).

Furthermore, Selwan teaches a first latch circuit 1212 that stores the display-data from the single-port memory 1210 in response to a first latch signal; and a second latch circuit 1214 that stores an output of the first latch circuit in response to a second latch signal, and wherein the controller 1210 outputs the first latch signal based on the second latch signal and a CPU-access signal that indicates the access operation of the CPU to the single-port memory (see figure 12 at 1210, 1212, 1214)

Regarding **claims 13-15**, in further discussion of claim 11, Selwan teaches how the display data is piped from the holding latch 1214 to the Pixel FIFO 1244 and based on the load signal from the FIFO control 1220 this display data is piped to the LCD/CRT via the Attribute Controller and the CRT interface (*see* figure 12).

However, Selwan does not teach how priority is given to CPU when the CPU has access to memory while data is being retrieved from the memory to the liquid crystal driver. On the other hand, Shimomura teaches a data processing system comprising: a CPU; a memory for storing programs and display data; a memory controller connected to said CPU via a CPU bus and said memory via a memory bus, **for providing priority** to an access request from said CPU to said memory, said memory controller having a display controller for reading the display data stored in said memory, and a buffer for storing an access request from said display controller to said memory, and execution of the memory access by said display controller in response to an access request from said CPU (column 34, lines 55-67).

Thus, it would have been obvious to combine Selwan and Shimomura because while Selwan teaches how a liquid crystal driver retrieves the display-data stored in the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section by teaching that when display memory read FIFO 1212 starts filling up, data is input into holding latch 1214 such that when holding latch 1214 has valid data in it, FIFO control circuit block 1220 clocks data into pixel FIFO 1244 and into Down Counter 1216 (see figure 19, lines 58 through column 20, line 2, figure 12), Shimomura teaches how priority is given to CPU when the CPU has access to memory by means of a memory controller connected to said CPU via a CPU bus and said memory via a memory bus, **for providing priority** to an access request from said CPU to said memory, said memory controller having a display controller for reading the display data stored in said memory, and a buffer for storing an access request from said display controller to said memory, and execution of the memory access by said display controller in response to an access request from said CPU (column 34, lines 55-67). The motivation for combining these inventions would have been to prevent performance degradation due to waiting of the CPU for access to the main memory (column 3, lines 11-16).

Furthermore, Shimomura teaches in FIG. 9, how the transfer time register 910, the transfer time (delay time) of the first command from the CPU bus 131 to the memory bus 135 which is generated by the memory interface circuit 152 of the memory controller 140 when access from the CPU 100 is generated while the memory bus 135 is used by the display controller 156 or the rendering processor 157 is registered (column 13, lines 45-53, figure 9).

Regarding **claim 16**, in further discussion of claim 11, Selwan teaches a first latch circuit 1212 that stores the display-data from the single-port memory 1210 in response to a first latch signal; and a second latch circuit 1214 that stores an output of the first latch circuit in response to a second latch signal, and wherein the controller 1210 outputs the first latch signal based on the second latch signal and a CPU-access signal that indicates the access operation of the CPU to the single-port memory (see figure 12 at 1210, 1212, 1214).

However, Selwan does not teach how priority is given to CPU when the CPU has access to memory while data is being retrieved from the memory to the liquid crystal driver. On the other hand, Shimomura teaches a data processing system comprising: a CPU; a memory for storing programs and display data; a memory controller connected to said CPU via a CPU bus and said memory via a memory bus, **for providing priority** to an access request from said CPU to said memory, said memory controller having a display controller for reading the display data stored in said memory, and a buffer for storing an access request from said display controller to said memory, and execution of the memory access by said display controller in response to an access request from said CPU (column 34, lines 55-67).

Furthermore, Shimomura teaches in FIG. 9, how the transfer time register 910, the transfer time (delay time) of the first command from the CPU bus 131 to the memory bus 135 which is generated by the memory interface circuit 152 of the memory controller 140 when access from the CPU 100 is generated while the memory bus 135 is used by the display controller 156 or the rendering processor 157 is registered (column 13, lines 45-53, figure 9).

Allowable Subject Matter

6. **Claims 9, 17** and **18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,119,207 to *Chee* for a low priority FIFO request assignment for DRAM access.

U.S. Patent 5,673,416 to *Chee et al* for a memory request and control unit including a mechanism for issuing and removing requests for memory access.

U.S. Patent 6,145,033 to *Chee* for a management of display FIFO requests for DRAM access.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

08/20/2004

DENNIS-DOON CHOW
PRIMARY EXAMINER